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PATENT APPLICATION

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Attorney Docket No.: 10005465-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Naffziger

Serial No.: 09/696,104 Examiner: Nguyen, L.

Filing Date: October 24, 2000 Group Art Unit: 2816

Title: STATIC TO DYNAMIC LOGIC INTERFACE CIRCUIT

AMENDMENT

THE COMMISSIONER OF PATENTS
Washington, DC 20231

Sir:

In response to the Office Action mailed March 28, 1997, please amend the application as follows:

IN THE SPECIFICATION:

PLEASE RE-WRITE PAGE 3, PARAGRAPH 2 (A.K.A LINES 9-21) AS FOLLOWS:

An embodiment of the invention uses standard clock signals, a delay element that can be as simple as a series of inverters, and an enabled latch to interface static logic to dynamic logic. The inverse of the dynamic logic evaluate clock is fed to the clock input of a transparent latch with clock and enable inputs. A delayed version of this clock is generated by the delay element. This delayed inverse of the dynamic logic evaluate clock is fed to the enable input of the latch. The input to the latch comes from static logic and the output of the latch is fed to the dynamic logic. The net result is a latch that is open until the evaluate clock is instructing the dynamic logic to evaluate and remains closed